Notice of Allowability	Application No.	Applicant(s)	
	10/632,241	ONG ET AL.	
	Examiner	Art Unit	
	Niketa I. Patel	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *After Final amendment filed on 9/4/2007*.

2. ☒ The allowed claim(s) is/are *1-5,7,9-12,15-20,22,24-27 and 30-36 (renumbered as 1-28)*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An extension of time under 37 CFR 1.136(a) is required in order to make an examiner's amendment which places this application in condition for allowance. During a telephone conversation conducted on 10/12/2007, examiner requested an extension of time for two MONTH(S) and authorized the Director to charge Deposit Account No. 02-2666 the required fee of $460.00 for this extension and authorized the following examiner's amendment. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

Note: underline text indicates new text being entered and strike through text indicates that the text is deleted from the claim.

AMENDMENTS TO THE CLAIMS

Claim 1. (Currently amended) A circuit comprising:

a first device coupled with a first bus, wherein the first device is not compliant with a PCI (peripheral component interconnect) standard, the first device containing operating system data, wherein the operating system data is not ~~operational for the circuit with a~~ bootable for any device that is not compliant with the PCI standard according to a system BIOS (basic input output system);

a second device coupled with a second bus, wherein the second device is

compliant with the PCI standard and the second bus is a PCI standard bus, the second device to be associated with the operating system data from the first device, the association of the second device with the operating system data from the first device enabling the operating system data from the first device to be ~~utilized~~ booted according to the PCI standard; and

a memory to receive the operating system data from the first device.

Claim 2. (Currently amended) The circuit of claim 1, further comprising a plurality of devices coupled with the second bus, wherein each of the plurality of devices is compliant with the PCI standard, and wherein the plurality of devices includes the second device.

Claim 3. (Currently amended) The circuit of claim 2, further comprising a controller coupled with the first bus and the second bus to scan the plurality of PCI standard devices to identify the second device.

Claim 4. (Original) The circuit of claim 1, wherein the second device comprises a function of a physical device.

Claim 5. (Original) The circuit of claim 1, wherein the first device comprises flash memory.

Claim 6. (Cancelled)

Claim 7. (Currently amended) The circuit of ~~claim 6~~ claim 1, wherein the operating system data includes a boot loader, the boot loader being stored as an option-ROM for the first device.

Claim 8. (Cancelled)

Claim 9. (Currently amended) A method comprising:

identifying a peripheral device that is coupled with a first bus, the peripheral device being a standard peripheral device according to a PCI (peripheral component interconnect) standard;

associating the standard peripheral device with operating system data of a non-standard peripheral device that is coupled with a second bus, wherein the operating system data is not ~~operational with a~~ bootable for any non-standard peripheral device according to a system BIOS (basic input output system); and

based on the association of the PCI standard peripheral device with the operating system data of the non-standard peripheral device, dispatching the operating system data of the non-standard peripheral device to memory as data in accordance with the PCI standard ~~of the standard peripheral device~~.

Claim 10. (Previously presented) The method of claim 9, wherein identifying the standard peripheral device comprises choosing the standard peripheral device from a plurality of standard peripheral devices that are coupled with the first bus.

Claim 11. (Original) The method of claim 10, wherein choosing the standard peripheral device comprises pre-selecting the standard peripheral device before commencing operations.

Claim 12. (Previously Presented) The method of claim 10, wherein choosing the standard peripheral device comprises scanning the plurality of standard peripheral devices coupled with the first bus to identify a suitable device.

Claim 13-14. (Cancelled)

Claim 15. (Currently amended) The method of ~~claim 14~~ claim 10, wherein the operating system data includes a boot loader, the boot loader being stored as an option-ROM.

Claim 16. (Currently amended) A computer system comprising:

a processor;

a first bus, the first bus being in compliance with a PCI (peripheral component interconnect) standard;

a first device that is not compliant with [[a]] the PCI standard, the first device being coupled with a second bus, the first device containing operating system data, wherein the operating system data is not ~~operational~~ bootable for the computer system with [[a]] any device that is not compliant with the PCI standard according to a BIOS (basic input output system) of the computer system;

a plurality of devices in compliance with the PCI standard, each of the plurality of devices being coupled with the ~~second~~ first bus, the plurality of devices including a second device to be associated with the operating system data from the first device, the processor recognizing the operating system data as being operating system data in accordance with the PCI standard because of the association of the second device with the operating system data; and

a memory to receive the operating system data from the first device.

Claim 17. (Original) The computer system of claim 16, wherein the computer system is an embedded system.

Claim 18. (Currently amended) The computer system of claim 16, further comprising a controller coupled with the first bus and the second bus to scan the plurality of devices in compliance with the PCI standard to identify the second device.

Claim 19. (Original) The computer system of claim 16, wherein the plurality of devices includes one or more functions of a physical device.

Claim 20. (Original) The computer system of claim 16, wherein the first device comprises flash memory.

Claim 21. (Cancelled)

Claim 22. (Previously presented) The computer system of claim 16, wherein a portion of the data is stored as an option-ROM for the first device.

Claim 23. (Cancelled)

Claim 24. (Currently amended) A ~~machine-readable~~ computer-readable storage medium having stored thereon data representing sequences of instructions that, when executed by a processor, cause the processor to perform operations comprising:

identifying a PCI (peripheral component interconnect) standard peripheral device on a first bus;

associating the PCI standard peripheral device with operating system data contained in a non-standard peripheral device, wherein the operating system data is not ~~operational with a~~ bootable for any non-standard peripheral device according to a system BIOS (basic input output system); and

based on the association of the PCI standard peripheral device with the operating system data of the non-standard peripheral, dispatching the operating system data of the non-standard device to memory as data in accordance with the PCI standard ~~of the standard peripheral device~~.

Claim 25. (Currently amended) The storage medium of claim 24, wherein identifying the PCI standard peripheral device comprises choosing the PCI standard peripheral device from a plurality of standard peripheral devices on the first bus.

Claim 26. (Currently amended) The storage medium of claim 25, wherein choosing the PCI standard peripheral device comprises pre-selecting the PCI standard peripheral device before commencing operations.

Claim 27. (Currently amended) The storage medium of claim 25, wherein choosing the PCI standard peripheral device comprises scanning the plurality of standard peripheral devices on the first bus to identify a suitable device.

Claim 28-29. (Cancelled)

Claim 30. (Currently amended) The storage medium of ~~claim 29~~ claim 24, wherein the operating system data includes a boot loader, the boot loader being stored as an option-ROM.

Claim 31. (Currently amended) The ~~apparatus~~ circuit of claim 3, further comprising a second controller coupled with the controller and the memory, wherein the memory receives the operating system data via the second controller.

Claim 32. (Previously presented) The method of claim 12, wherein the scanning of the plurality of standard peripheral devices is performed by a first controller that is coupled with the first bus and the second bus.

Claim 33. (Currently amended) The method of claim 32, wherein the dispatching of the operating system data to memory comprises transferring the operating system data to memory via a second controller that is coupled with the memory and the first controller.

Claim 34. (Currently amended) The computer system of claim 18, further comprising a second controller coupled with the controller and the memory, wherein the memory receives the operating system data via the second controller.

Claim 35. (Currently amended) The storage medium of claim 25, wherein the choice of the PCI standard peripheral devices from the plurality of standard peripheral devices is performed by a first controller that is coupled with the first bus and the second bus.

Claim 36. (Currently amended) The ~~method~~ storage medium of claim 35, wherein the dispatching of the operating system data to memory comprises transferring the operating system data to memory via a second controller that is coupled with the memory and the first controller.

AMENDMENT TO TITLE

SUPPORT FOR NON-STANDARD DEVICE CONTAINING OPERATING SYSTEM DATA

AMENDMENTS TO SPECIFICATION

SUPPORT FOR NON-STANDARD DEVICE CONTAINING OPERATING SYSTEM DATA

[0010] A method and apparatus are described for provision of support for a non-standard device containing operating system data.

AMENDMENTS TO ABSTRACT

According to an embodiment of the invention, a method and apparatus for support of a non-standard device containing operating system data are described. According to one

embodiment, a circuit comprises a first device that is not compliant with a PCI (peripheral component interconnect) standard, the first device containing operating system data, where the operating system data is not bootable for any non-standard device; a second device that is compliant with the PCI standard, the second device being ~~a temporary target for~~ associated with the operating system data, the association of the second device with the operating system data from the first device enabling the operating system data from the first device to be booted according to the PCI standard; and a memory to receive the operating system data from the first device.

2. The following is an examiner's statement of reasons for allowance: the prior art of record taken alone and/or in combination with other does not teach the limitation of a first device not compliant with PCI standard, containing operating system data, wherein the operating system data is not bootable for any device that is not compliant with the PCI standard according to a system BIOS and a second device, that is compliant with the PCI standard and the second device to be associated with the operating system data from the first device, the association of the second device with the operating system data from the first device enabling the operating system data from the first device to be booted according to the PCI standard, in combination with other recited limitations.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Niketa I. Patel whose telephone number is (571) 272 4156. The examiner can normally be reached on M-F 8:00 A.M. to 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272 4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Niketa Patel
Patent Examiner
10/12/2007